ECE 4170: Introduction to HDL with Applications to Digital System Design

School of Electrical and Computer Engineering
Georgia Institute of Technology
Spring 2007 Semester
Instructor: Prof. Sudhakar Yalamanchili

Template for Project Report

Submission Date: April 27th 2007 (there will be no extensions)

Have Questions?: Please e-mail or meet TA

Your final report will have two components - your VHDL source and the report.

1 VHDL Source

Create a zip file of your VHDL source. The top level directory should contain a README that describes

1. Directory structure
2. Instructions for compiling and testing for i) simulation, and ii) synthesis.
3. If the project in its entirety does not work, identify those components that do work and how they can be tested. This is something you should be documenting as you develop you design (not much additional work for the final report) rather than something you try and complete after you are done (a great deal of work for the final report).

2 The Final Report

The final report should have the following sections. All page counts are upper bounds – you can have less.

1. Introduction (2 pages): Describe the original goal of the project, the realized goal of the project, and accompany it with a block diagram. Include a Final Status table that lists all major design entities and indicates its status as COMPLETE (simulated and synthesized designs function correctly), SIMULATION_OK (i.e., synthesized design not validated) or SYNTHESIS_OK.
2. Functionality (3 pages): The project implementation in sufficient detail. This reflects your understanding after having completed the project. The details should include low level details such as bit widths, timing, pipeline stages, etc. Use of figures is highly encouraged. Brevity is important. You are now describing results and not how you will perform a design.
3. Evaluation (2 pages): Report on characteristics of the design. For the simulation modeling, report on run-times, physical characteristics of your implementation (approximate lines of code and number of design entities) and simulation run

times (e.g., where they excessively long). For synthesis report at least area and maximum clock frequency. Table formats are encouraged.

4. Lessons Learned: This section has two subsections.
    a. If you had to repeat this design what would you do differently?
    b. What generic lessons have you learned, misconceptions dispelled, or insights acquired?

3 Evaluation

The final project grading will be broken down as follows: Simulation 75% and Synthesis 25%. Note that you do receive partial credit for modules that do synthesize and/or simulate correctly even if you overall project has not been completed in its entirety.

4 Submission

Email to the instructor and copy the TA. Submission deadline – Friday, April 27th, 9pm.